UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,844	09/28/2006	Akira Ohuchi	Q97404	3674

23373 7590 11/12/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
HARRISTON, WILLIAM A	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,844	OHUCHI ET AL.	
	Examiner	Art Unit	
	WILLIAM HARRISTON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-9, 11 and 12* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement filed 9/28/2006 has been considered.

Oath/Declaration

3. The oath or declaration filed on 9/28/2006 is acceptable.

Drawings

4. The drawings filed on 9/28/2006 are acceptable.

Specification

5. The abstract of the disclosure and the specification filed on 9/28/2006 are acceptable.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4, 6-9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qi et al. (US 6774497 B1) taken with Fujimori et al (US 2004/0046252 A1). Examiner notes that the '497 references expresses units of length in "mils". 1 mil ≈ 25.4μm.

9. Regarding claim 1, figure 2b of Qi et al. disclose a semiconductor device (200) comprising a wiring board (240) in which electrode pads (242) are formed on the surface thereof, a semiconductor element (210) which is disposed on the wiring board and in which electrodes (214) are formed on the surface thereof, bumps (220) for connecting said electrodes to said electrode pads, said bumps being formed from solder, and an underfill material (230) filled between said wiring board and said semiconductor element to embed said bumps, wherein said wiring board comprises a solder resist (250) disposed on the surface of the side on which said electrode pads are formed, wherein apertures for exposing said electrode pads are formed on the solder resist (Examiner has interpreted "apertures" to be openings formed in the solder resist layer, this feature is disclosed at column 6, line 49-51) and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill resin disposed on said solder resist in said area between said wiring board a said semiconductor element. See column 7.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). One of ordinary skill in the

art would be motivated to form an underfill material from resin for the purpose of reducing heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

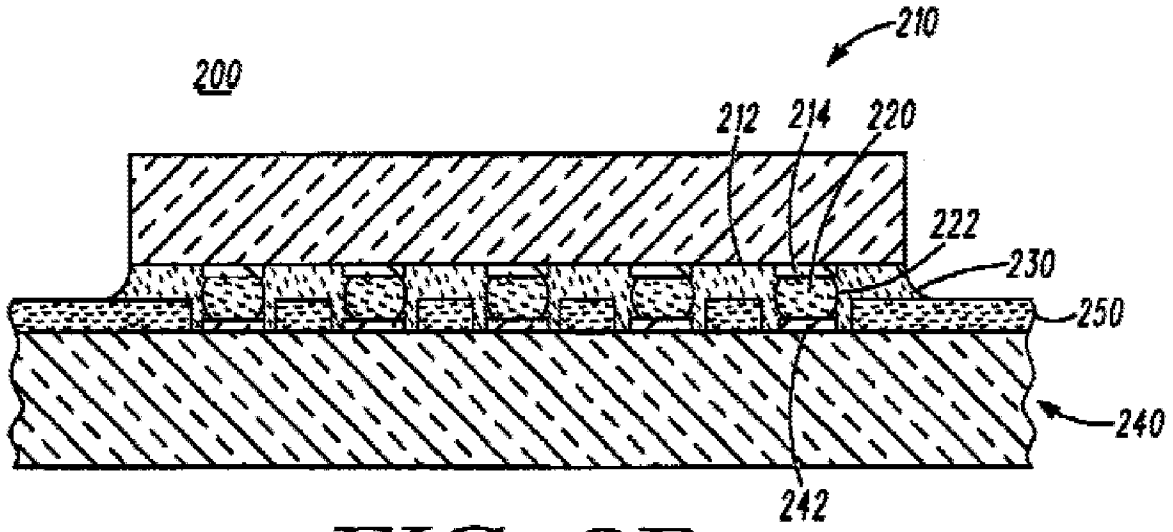

FIG. 2B

10. Regarding claim 2, Qi et al. taken with Fujimori et al. disclose the device of claim 1 for the reasons stated above. Qi et al. further disclose the device wherein the thickness of said underfill resin disposed on said solder resist is 50 micrometers or less. See Qi et al. column 7, lines 1-6.

11. Regarding claim 3, Qi et al. taken with Fujimori et al. disclose the device of claim 1 for the reasons stated above. Qi et al. do not disclose the device wherein the volume of said bumps is less than the volume of said apertures. However, it is known in the art that forming an aperture having a small volume causes air bubbles to be trapped in an

underfill material. The trapped air bubbles cause voids to be generated in the underfill material, thus reducing its reliability. One of ordinary skill in the art would be motivated to form said apertures with a greater volume than said bumps to avoid air bubbles being trapped in an underfill material.

12. Regarding claim 4, Qi et al. taken with Fujimori et al. disclose the device of claim 3 for the reasons stated above. Qi et al. further disclose the device wherein the thickness of said solder resist (250) is 30 micrometers or more. See Qi et al. column 6 lines 60-62.

13. Regarding claim 6, figures 1-3 of Qi et al. disclose a method for manufacturing a semiconductor device comprising the steps of forming bumps (120) on at least one element selected from said electrode pads(114) and said electrodes (242) (310), depositing an underfill material (130) on at least a portion of the area in which said semiconductor element (110) is to be mounted on said wiring board (240) (320), pressing said semiconductor element to said wiring board to connect said electrode pads, said bumps, and said electrodes to each other, melting and then solidifying said bumps to join said electrodes to said electrode pads by way of said bumps, and curing said resin material and forming an underfill resin so that said bumps become embedded between said wiring board and said semiconductor element, wherein the distance between said wiring board and said semiconductor element is controlled during the melting of said bumps in said joining step, and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill material disposed on said solder resist in said area

between said wiring board and said semiconductor element after said underfill material has been formed. See columns 7 and 8.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). One of ordinary skill in the art would be motivated to form an underfill material from resin for the purpose of reducing heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes. one of ordinary skill in the art would be motivated to form an underfill material from resin because its use is well known in the art.

14. Regarding claim 7, Qi et al. taken with Fujimori et al. disclose the method of claim 6 for the reasons stated above. Qi et al. do not disclose the method wherein the volume of said bumps is less than the volume of said apertures. However, it is known in the art that forming an aperture having a small volume causes air bubbles to be trapped in an underfill material. The trapped air bubbles cause voids to be generated in the underfill material, thus reducing its reliability. One of ordinary skill in the art would be motivated to form said apertures with a greater volume than said bumps to avoid air bubbles being trapped in an underfill material.

15. Regarding claim 8, Qi et al. taken with Fujimori et al. disclose the method of claim 7 for the reasons stated above. Qi et al. further disclose the method wherein the thickness of said solder resist (250) is 30 micrometers or more. See column 6.

16. Regarding claim 9, Qi et al. taken with Fujimori et al. disclose the method of claim 8 for the reasons stated above. Qi et al. further disclose the method wherein the distance between said wiring board and semiconductor element is controlled by controlling the relative position of said semiconductor element with respect to said wiring board in said joining step. See column 7.

17. Regarding claim 11, Qi et al. taken with Fujimori et al. disclose the method of claim 6 for the reasons stated above. Qi et al. further disclose an underfill material to which a chemical capable of removing an oxide film is added is used as an underfill material. See column 7, line 52- column 8.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). One of ordinary skill in the art would be motivated to form an underfill material from resin for the purpose of reducing heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes. one of ordinary skill in the art would be motivated to form an underfill material from resin because its use is well known in the art.

18. Regarding claim 12, Qi et al. taken with Fujimori et al. disclose the device of claim 6 for the reasons stated above. Qi taken with Fujimori no dot disclose the step of carrying out a plasma treatment. However, plasma treatment is well known in the art for growing largely crystalline oxide coating, which present high hardness and a continuous

barrier, on metals. One of ordinary skill in the art would be motivated to perform a plasma treatment for the purpose of offering protection against wear, corrosion, and heat.

Conclusion

19. JP 2002-256288 is made of record and not relied upon, yet is considered pertinent to applicant's disclosure. This document is cited for disclosing a resin underfill material, and for further disclosing the problems caused by having apertures with a small volume. US 2005/0155790 was used as an English translation of JP 2002-256288.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM HARRISTON whose telephone number is (571)270-3897. The examiner can normally be reached on Monday - Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. H./
Examiner, Art Unit 2826

/Sue A Purvis/
Supervisory Patent Examiner, Art Unit 2826